In the Claims:

1. (Original) A multi-layer semiconductor wafer structure defining a multiplicity of dies formed thereon, said wafer structure comprising:

a first scribe line having a selected width extending along a first direction and adjacent a first die of said multiplicity of dies;

a second scribe line having a selected width extending along a second direction adjacent said first die and intersecting said first scribe line at a corner point of said first die;

at least one free area defined on at least one of said first and second scribe lines where placement of a test key is restricted.

2. (Original) The multi-layer semiconductor wafer structure of claim 1 wherein at least one layer of said wafer structure is a low-k dielectric layer.

3. (Previously Presented) The multi-layer semiconductor wafer structure of claim 2 wherein the low-k dielectric layer has a dielectric constant of less than approximately 3.5.

4. (Original) The multi-layer semiconductor wafer structure of claim 3 wherein the low-k dielectric layer has a dielectric constant of less than 3.0.

5. (Currently Amended) The multi-layer semiconductor wafer structure of claim 2 wherein the low-k dielectric layer is a material selected from the group consisting of CVD-SiOC, SiOCN, Spin-on SiOC, CVD deposited polymer, Spin-on polymer, FSG, SiO_2 and combinations thereof.

6. (Previously Presented) The multi-layer semiconductor wafer structure of claim 1 wherein said free area is a free area A_1 on the first scribe line and is defined by the equation $A_1=D_1xS_1$ where D_1 is the distance along the first direction extending from the corner point of the first die, and S_1 is the width of the first scribe line.

7. (Previously Presented) The multi-layer semiconductor wafer structure of claim 1 wherein the free area is defined on the top layer of the multi-layer structure.

8. (Original) The multi-layer semiconductor wafer structure of claim 1 wherein the free area is defined on at least one of the top three layers of the multi-layer structure.

9. (Original) The multi-layer semiconductor wafer structure of claim 6 further comprising at least one test key formed in said free area, said at least one test key having a measurement ratio R_1, wherein the measurement ratio is defined by the equation: $R_1=M_1/A_1$, wherein M_1 is the total area of said at least one test key formed on the free area A_1, and R_1 is less than about 10%.

10. (Original) The multi-layer semiconductor wafer structure of claim 6 wherein the distance D_1 is less than about 600μm.

11. (Original) The multi-layer semiconductor wafer structure of claim 6 wherein the width S_1 of the first scribe line is greater than about 20μm.

12. (Original) The multi-layer semiconductor wafer structure of claim 1 wherein the multi-layer structure is formed on a substrate selected from the group consisting of bulk Si, SOI, SiGe, GaAs, InP, and a combination thereof.

13. (Previously Presented) The multi-layer semiconductor wafer structure of claim 1 wherein said first die comprises:

a first peripheral region inside of and extending parallel to said first scribe line;

a second peripheral region inside of and extending parallel to said second scribe line and intersecting said first peripheral region to form a corner area;

a conductive ring formed between said first die and said first peripheral region and said second peripheral region; and

an array of apertures formed in the conductive ring and adjacent the corner area of the first die.

14. (Original) The multi-layer semiconductor wafer structure of claim 13 wherein said array of apertures comprises at least two slots.

15. (Original) The multi-layer semiconductor wafer structure of claim 13 wherein said array of apertures comprises two rows of holes.

16. (Original) The multi-layer semiconductor wafer structure of claim 13 wherein the array of apertures extends along at least one of the first peripheral region and the second peripheral region.

17. (Previously Presented) The multi-layer semiconductor wafer structure of claim 13 wherein the first die further comprises a circuit area with a plurality of circuit elements, wherein the conductive ring is electrically connected to the circuit elements to apply one of a power source and a ground potential to the circuit elements.

18. (Original) The multi-layer semiconductor wafer structure of claim 13 wherein the conductive ring has a width of between 50μm and about 300μm.

19. (Original) The multi-layer semiconductor wafer structure of claim 1 wherein said free area is a free area A_S at the intersection of said first scribe line and said second scribe line and is defined by the equation $A_S=S_1xS_2$, wherein S_1 is the width of the first scribe line and S_2 is the width of the second scribe line.

20. (Original) The multi-layer semiconductor wafer structure of claim 19 further comprising at least one test key formed on said free area A_S, said test key having a measurement ratio R_S that is less than 10% and is defined by the equation $R_S=M_S/A_S$, wherein M_S is the total area of said at least one test key formed on the free area A_S.

21. (Original) The multi-layer semiconductor wafer structure of claim 19 wherein the width of the scribe lines S_1 and S_2 is greater than about 20μm.

22. (Original) The multi-layer semiconductor wafer structure of claim 1 wherein said at lest one free area comprises a first free area A_1 on the first scribe line and a second free area A_2 on

the second scribe line, said first free area defined by the equation $A_1=D_1xS_1$ where D_1 is the distance along the first direction extending from the corner point of the die and S_1 is the width of the first scribe line, said second free area defined by the equation $A_2=D_2xS_2$ where D_2 is the distance along the second direction extending from the corner point of the die and S_2 is the width of the second scribe line.

23. (Original) The multi-layer semiconductor wafer structure of claim 22 comprising a third free area A_S at the intersection of said first scribe line and said second scribe line and is defined by the equation $A_S=S_1xS_2$.

24. (Previously Presented) The multi-layer semiconductor wafer structure of claim 23 further comprising:

at least one test key formed on at least one of the free areas A_1, A_2 and A_S;

wherein a first measurement ratio R_1 is defined as the equation $R_1=M_1/A_1$, wherein M_1 is the total area of the test keys formed on the first free area A_1;

wherein a second measurement ratio R_2 is defined as the equation $R_2=M_2/A_2$, wherein M_2 is the total area of the test keys formed on the second free area A_2;

wherein a third measurement ratio R_S is defined as the equation $R_S=M_S/A_S$, wherein M_S is the total area of the test keys formed on the third area A_S; and

wherein a total measurement ratio R is defined as the equation $R=(M_1+M_2+M_S) / (A_1+A_2+A_S)$.

25. (Original) The multi-layer semiconductor wafer structure of claim 24 wherein R_1 is less than about 10%.

26. (Original) The multi-layer semiconductor wafer structure of claim 24 wherein R_2 is less than about 10%.

27. (Original) The multi-layer semiconductor wafer structure of claim 24 wherein R_S is less than about 10%.

28. (Original) The multi-layer semiconductor wafer structure of claim 24 wherein the ratio R is less than about 10%.

29. (Previously Presented) The multi-layer semiconductor wafer structure of claim 22 wherein the first distance D_1 is less than about 600μm.

30. (Previously Presented) The multi-layer semiconductor wafer structure of claim 22 wherein the distance D_2 along the second direction is less than about 600μm.

31. (Previously Presented) The multi-layer semiconductor wafer structure of claim 22 wherein the width S_1 of the first scribe line is greater than about 20μm.

32. (Previously Presented) The multi-layer semiconductor wafer structure of claim 22 wherein the width S_2 of the second scribe line is greater than about 20μm.

33. (Original) A multi-layer semiconductor wafer structure defining a multiplicity of dies formed thereon, said wafer structure comprising:

a first scribe line having a selected width extending along a first direction;

a second scribe line having a selected width extending along a second direction and intersecting said first scribe line;

four dies located at and separated by the intersection of said first and second scribe lines wherein each of the four dies comprises a corner point adjacent the intersection of said first and second scribe lines;

a first free area A_1 on the first scribe line adjacent the corner point of the first die, wherein A_1 is defined by the equation $A_1=D_1xS_1$ and wherein D_1 is the distance extending from the corner point of the first die, and S_1 is the width of the first scribe line;

a second free area A_2 on the second scribe line adjacent the corner point of the second die, wherein A_2 is defined by the equation $A_2=D_2xS_2$, and wherein D_2 is the distance from the corner point of the second die, and S_2 is the width of the second scribe line;

a third free area A_3 on the second scribe line adjacent the third corner point of the third die, wherein A_3 is defined by the equation $A_3=D_3xS_2$, and wherein D_3 is the distance from the corner point of the third die;

a fourth free area A_4 on the first scribe line adjacent the corner point of the fourth die, wherein A_4 is defined by the equation $A_4=D_4xS_1$, and wherein D_4 is the distance from the corner point of the fourth die; and

a fifth free area A_5 on the intersection of the first scribe line and the second scribe line and is defined by the equation $A_5=S_1xS_2$.

34. (Original) The semiconductor wafer of claim 33 further comprising:

at least one test key formed on at least one of the free areas A_1, A_2, A_3, A_4 and A_S;

wherein a first measurement ratio R_1 is defined as the equation $R_1=M_1/A_1$, wherein M_1 is the total area of the test keys formed on the first free area A_1;

wherein a second measurement ratio R_2 is defined as the equation: $R_2= M_2/A_2$, wherein M_2 is the total area of the test keys formed on the second free area A_2;

wherein a third measurement ratio R_3 is defined as the equation: $R_3= M_3/A_3$, wherein M_3 is the total area of the test keys formed on the third free area A_3;

wherein a fourth measurement ratio R_4 is defined as the equation: $R_4= M_4/A_4$, wherein M_4 is the total area of the test keys formed on the fourth free area A_4;

wherein a fifth measurement ratio R_S is defined as the equation: $R_S= M_S/A_S$, wherein M_S is the total area of the test keys formed on the fifth free area A_S; and

wherein a total measurement ration R is defined as the equation $R=(M_1+M_2+M_3+M_4+M_S) / (A_1+A_2+A_3+A_4+A_S)$.

35. (Original) The semiconductor wafer of claim 34 wherein the first measurement ratio R_1 is less than about 10%.

36. (Original) The semiconductor wafer of claim 33 wherein the distance D_4 is less than about 600μm.

37. (Original) The semiconductor wafer of claim 33 wherein the width S_1 of the first scribe line is greater than about 20μm.

38. (Original) The semiconductor wafer of claim 33 wherein the width S_2 of the second scribe line is greater than about 20μm.

39. (Original) The semiconductor wafer of claim 33 wherein the multi-layer structure is formed on a substrate selected from the group consisting of bulk Si, SOI, SiGe, GaAs and InP.

40. (Original) The semiconductor wafer of claim 33 wherein each of said four dies comprises:

a first peripheral region parallel to said first scribe line;

a second peripheral region parallel to said second scribe line;

a conductive ring formed between said die and said first peripheral region and said second peripheral region; and

an array of apertures formed in the conductive ring and adjacent the corner area of the die.

41. (Previously Presented) The semiconductor wafer of claim 33 wherein at least one layer of the multilayered wafer structure is a low-k dielectric layer-having a dielectric constant less than approximately 3.5.

42. (Original) The semiconductor wafer of claim 40 wherein the array of apertures comprises two rows of holes.

43. (Original) The semiconductor wafer of claim 41 wherein said array of apertures comprises at least two slots.

44. (Original) The semiconductor wafer of claim 40 wherein the array of apertures extends along at least one of the first peripheral region and the second peripheral region.

45. (Original) The semiconductor wafer of claim 40, wherein each of the four dies further comprises a circuit area with a plurality of circuit elements, wherein the conductive ring is electrically connected to the circuit elements to apply one of a power source and a ground potential to the circuit elements.

46. (Original) The semiconductor wafer of claim 40 wherein the conductive ring has a width of between about 50μm and 300μm.

47. (Withdrawn) A fabrication method for a multi-layer semiconductor wafer defining a multiplicity of dies, the fabrication method comprising the steps of:

providing a semiconductor wafer having a first and second scribe line, wherein a corner point of a die is defined by an intersection of the first scribe line and the second scribe line;

defining a free area where the placement of test keys is restricted, the free area being located on the first scribe line adjacent the corner point of the die; and

cutting through the first scribe line and the second scribe line to separate the die.

48. (Withdrawn) The method of claim 47 wherein said step of cutting is a method selected from the group consisting of diamond sawing, laser cutting, liquid jet scribing, water jet cutting and combinations of said cutting methods.

49. (Withdrawn) The method of claim 47 wherein at least one layer of the multilayered wafer structure is a low-k dielectric layer having a dielectric constant less than approximately 3.5.

50. (Withdrawn) The method of claim 49 wherein the low-k dielectric layer is selected from the group consisting of CVD, SiOC, SiOCN, Spin-on SiOC, CVD polymer, Spin-on polymer, FSG and SiO_2.

51. (Withdrawn) The method of claim 47 wherein said free area is the free area A_1 on the first scribe line and is defined by the equation $A_1=D_1xS_1$, where D_1 is the distance along a first direction extending from the corner point of the die and S_1 is the width of the first scribe line.

52. (Withdrawn) The method of claim 51 further comprising the step of forming at least one test key on the free area A_1 prior to said cutting step and wherein a measurement ratio R_1 is defined by the equation $R_1=M_1/A_1$, wherein M_1 is the total area of said at least one test key formed on the free area A_1, and wherein R_1 is less than about 10%.

53. (Withdrawn) The method of claim 51 wherein the distance D_1 is less than about 600μm.

54. (Withdrawn) The method of claim 51 wherein the width S_1 of the first scribe line is greater than about 20μm.

55. (Withdrawn) The method of claim 47 comprising the step of forming the multi-layer structure on a substrate selected from a group of materials consisting of bulk Si, SOI, SiGe, GaAs and InP.

56. (Withdrawn) The method of claim 47 further comprising the steps of:

defining a first peripheral region inside of and extending parallel to said first scribe line;

defining a second peripheral region inside of and extending parallel to said second scribe line;

forming a conductive ring between said die and said first peripheral region and said second peripheral region; and

forming an array of apertures in the conductive ring and adjacent the corner point of the die.

57. (Withdrawn) The method of claim 56 wherein the step of forming an array of apertures comprises the step of forming at least two slots.

58. (Withdrawn) The method of claim 56 wherein the step of forming an array of apertures comprises the step of forming at least two rows of holes.

59. (Withdrawn) The method of claim 56 further comprising the steps of connecting said conductive ring to circuit elements in said die and connecting a terminal of a source of power to said conductive ring.

60. (Withdrawn) The method of claim 59 further comprising the step of forming at least one test key on the free area A_S prior to said cutting step and wherein a measurement ratio R_S is defined by the equation $R_S=M_S/A_S$, wherein M_S is the total area of said at least one test key formed on the free area A_S, and wherein R_S is less than about 10%.

61. (Withdrawn) The method of claim 59 wherein the first scribe line has a width S_1 greater than about 20μm.

62. (Withdrawn) The method of claim 59 wherein the second scribe line has a width S_2 greater than about 20μm.

63. (Withdrawn) The method of claim 47 wherein said free area is the free area A_S at the intersection of the first scribe line and the second scribe line and is defined by the equation $A_S=S_1xS_2$, where S_1 is the width of the first scribe line and S_2 is the width of the second scribe line.

64. (Withdrawn) The method of claim 63 wherein said step of forming a free area further comprises forming the free area A_1 on the first scribe line and the free area A_2 on the second scribe line, said free area A_1 defined by the equation $A_1=D_1xS_1$, where D_1 is the distance along the first direction extending from the corner point of the die and said free area A_2 defined by the equation $A_2=D_2xS_2$ where D_2 is the distance along the second direction extending from the corner point of the die.